TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC74AP, TC74HC74AF, TC74HC74AFN

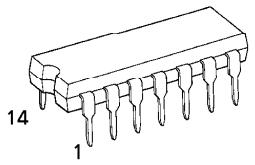
DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

(Note) The JEDEC SOP (FN) is not available in Japan.

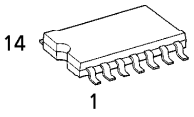
The TC74HC74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.
$\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

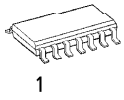
- High Speed ····· f_{MAX} = 77MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 2μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS74



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

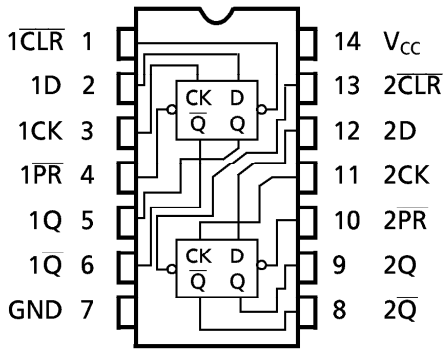


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

PIN ASSIGNMENT



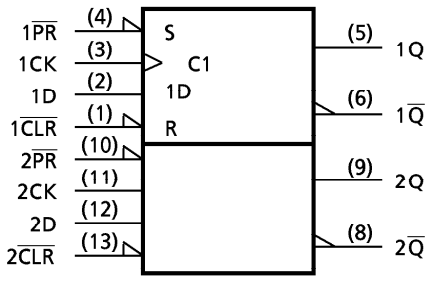
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

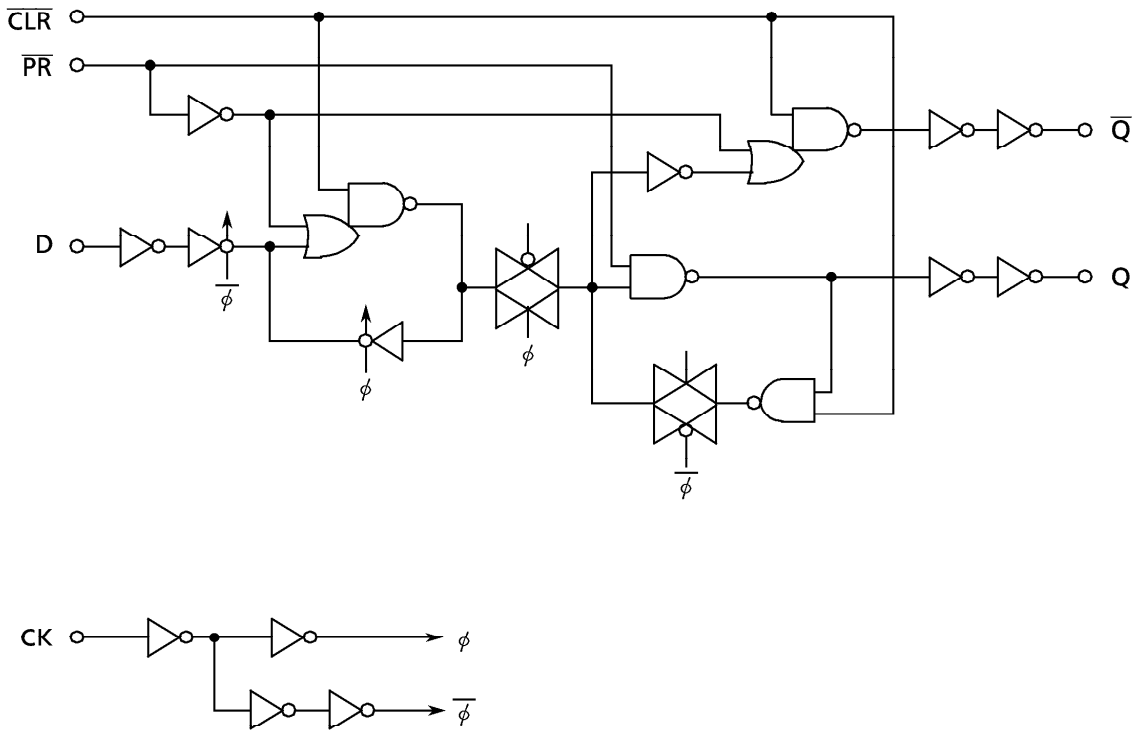
X : Don't Care

IEC LOGIC SYMBOL



961001EBA2

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Set−up Time	t_s		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Hold Time	t_h		2.0 4.5 6.0	− − −	0 0 0	0 0 0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0 4.5 6.0	− − −	25 5 4	30 6 5	
Clock Frequency	f		2.0 4.5 6.0	− − −	6 31 36	5 25 29	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	14	26	
Maximum Clock Frequency	f_{MAX}		36	77	−	MHz

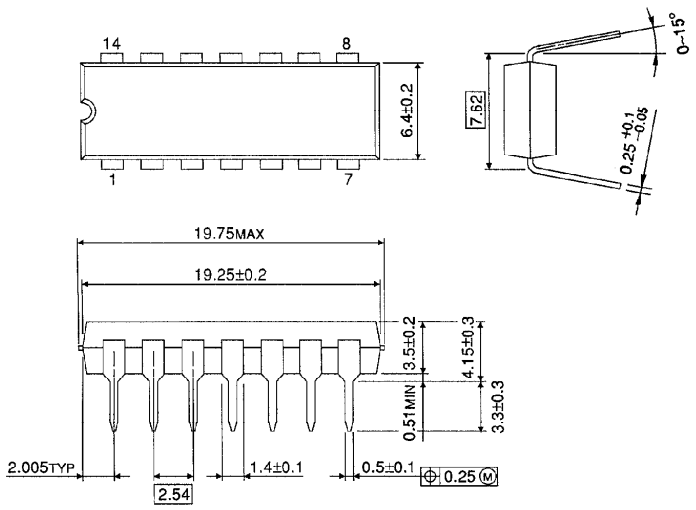
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	− − −	30 8 7	75 15 13	− − −	95 19 16	ns
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	− − −	48 16 13	150 30 26	− − −	190 38 32	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	− − −	51 17 15	150 30 26	− − −	190 38 32	
Maximum Clock Frequency	f_{MAX}		2.0 4.5 6.0	6 31 36	21 63 67	− − −	5 25 29	− − −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}	(1)		−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

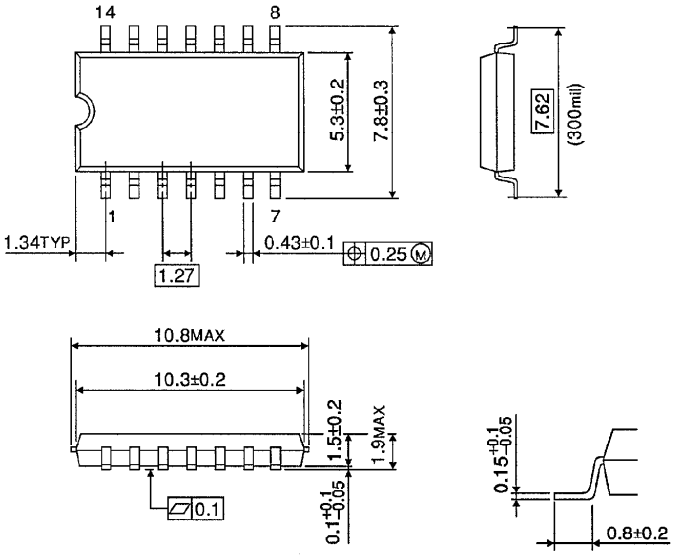
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per F / F)}$$

DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

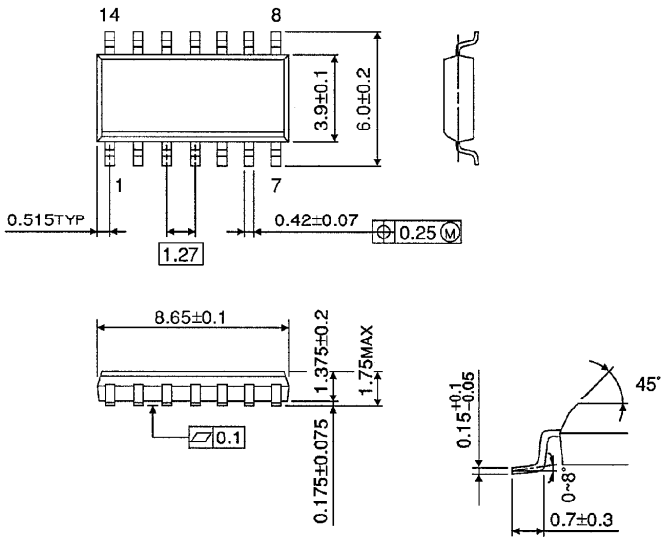
SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)